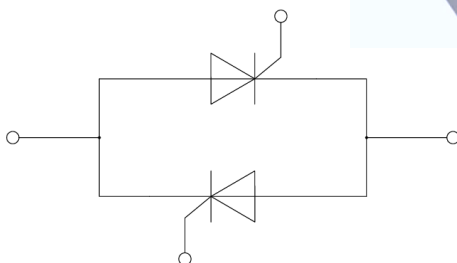
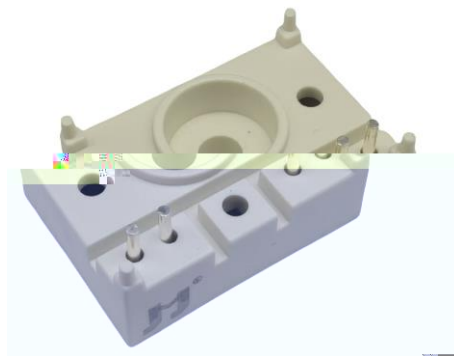




- A package consists of two inverse parallel SCR chips
- Welding by vacuum welding technology, which provide high reliability
- Insulated by silicone gel, provide a insulation voltage of 3000V~

V_{RRM}	1800	V
$I_{T(RMS)}(@ T_C = 80^{\circ}C)$	72	A
$I_{TSM}(@ t_P = 10ms)$	700	A
$V_T(Max)$	1.80	V

- Soft start
- Solid state relay
- AC/DC switch
- Temperature control



(@ $T_C = 25^{\circ}C$ unless otherwise specified)

Repetitive peak off-state voltage	$T_{vj} = 25^{\circ}C$	V_{DRM}	1800	V
Repetitive peak reverse voltage	$T_{vj} = 25^{\circ}C$	V_{RRM}	1800	V
Non-repetitive peak off-state voltage	$T_{vj} = 25^{\circ}C$	V_{DSM}	1900	V
Non-repetitive peak reverse voltage	$T_{vj} = 25^{\circ}C$	V_{RSM}	1900	V
RMS on-state current	$T_C = 80^{\circ}C$	$I_{T(RMS)}$	72	A
Forward surge current	1/2 cycle, Sine wave, 50Hz $T_{vj} = 25^{\circ}C$	I_{TSM}	700	A
I^2t value for fusing		I^2t	2450	A^2s
Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$	di/dt	150	$A/\mu s$
RMS isolation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3000/2500	V
Junction temperature range		T_J	-40 ~ +125	$^{\circ}C$
Storage temperature range		T_{stg}	-40 ~ +125	$^{\circ}C$



(@ $T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Peak forward voltage	$I_T=120\text{A}$, $t_P=380\mu\text{s}$	V_T			1.80	V
Repetitive peak off-state current	$V_D = V_{\text{DRM}}$, $T_{vj} = 25\text{ }^{\circ}\text{C}$	I_{DRM}			50	μA
	$V_D = V_{\text{DRM}}$, $T_{vj} = 125\text{ }^{\circ}\text{C}$				15	mA
Reverse leakage current	$V_R = V_{\text{RRM}}$, $T_{vj} = 25\text{ }^{\circ}\text{C}$	I_{RRM}			50	μA
	$V_R = V_{\text{RRM}}$, $T_{vj} = 125\text{ }^{\circ}\text{C}$				15	mA
Threshold voltage	For power loss calculation only $T_{vj} = 125\text{ }^{\circ}\text{C}$,	V_{TO}			0.9	V
Dynamic resistance	$T_{vj} = 125\text{ }^{\circ}\text{C}$,	r_T			8	m Ω
Triggering gate current	$V_D=12\text{V}$ $R_L=30\Omega$	I_{GT}	20		120	mA
Holding current	$I_T=1\text{A}$	I_H			150	mA
Latching current	$I_G=1.2 I_{\text{GT}}$	I_L			250	mA
Critical rate of rise of voltage	$V_D=2/3V_{\text{DRM}}$ $T_{vj}=125\text{ }^{\circ}\text{C}$ Gate Open	dv/dt	1000			V/ μs
Triggering gate voltage	$V_D=12\text{V}$ $R_L=30\Omega$	V_{GT}			1.5	V
Non triggering gate voltage	$V_D=V_{\text{DRM}}$ $T_{vj}=125\text{ }^{\circ}\text{C}$	V_{GD}	0.2			V

(@ $T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Thermal resistance, junction to case	per Thyristor	$R_{\text{th(j-c)}}$		0.8		/W
Mounting torque	Module torque to heatsink	M		1.5		N m

JMT72KQ18S1C	JMT72KQ18S1C	S1	10.6g/PCS	120 PCS	1080 PCS

FIG.1: Forward characteristics(per thyristor)

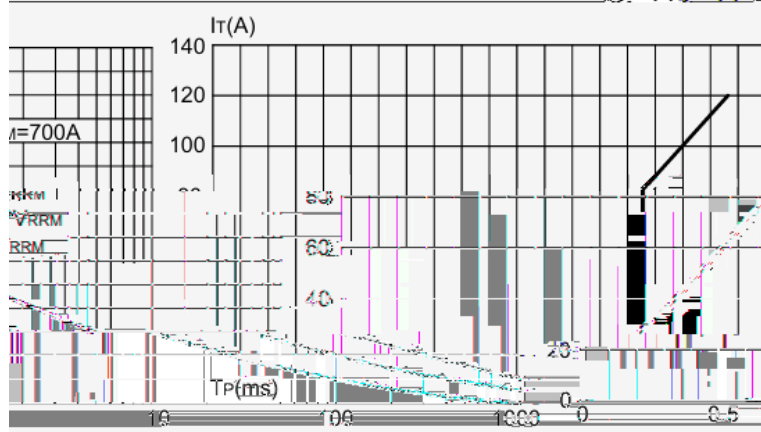


FIG.2: Surge overload current vs. time

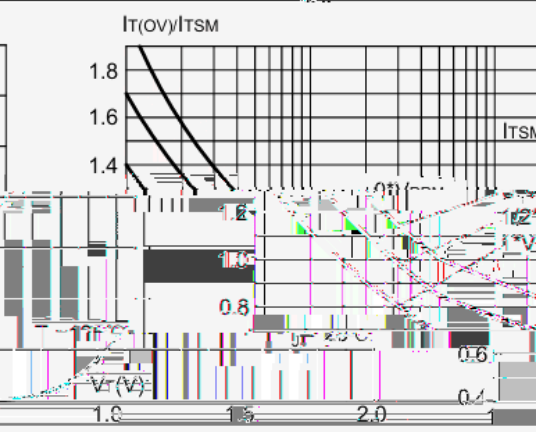


FIG.3: Power dissipation per module vs. R.M.S. current

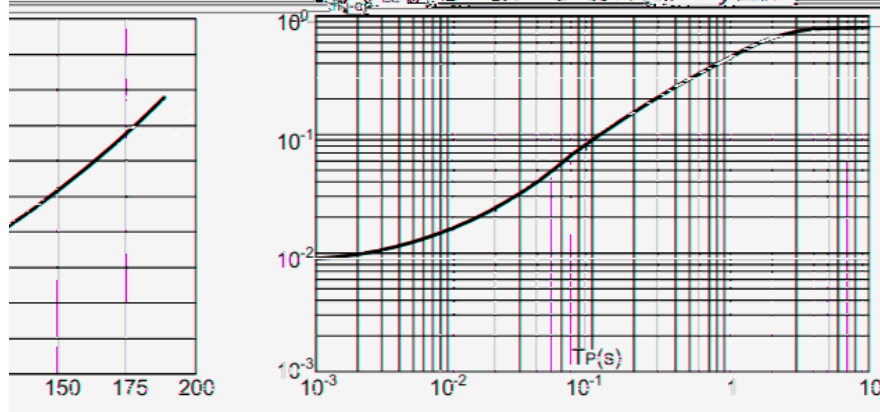


FIG.4

