

**XTgheXf****CdbWhVgFh Td**

- A package consists of four dual anti-parallel SCR chips
- Welding by vacuum welding technology, which provide high reliability
- Insulated by silicone gel, provide a insulation voltage of 3000V~

cc VTgbaf

- Soft start
- Solid state relay
- AC/DC switch
- Temperature control

Uf b hgX Tk h ETga f (@ T_C = 25 °C unless otherwise specified)

CTeT XgXe	6baWgbaf	FI Ub	I T hXf	Ha g
Repetitive peak off-state voltage	Tvj = 25 °C	V _{DRM}	1600	V
Repetitive peak reverse voltage	Tvj = 25 °C	V _{RRM}	1600	V
Non-repetitive peak off-state voltage	Tvj = 25 °C	V _{DSM}	1700	V
Non-repetitive peak reverse voltage	Tvj = 25 °C	V _{RSM}	1700	V
RMS on-state current	T _C = 80 °C	I _{T(RMS)}	50	A
Forward surge current	1/2 cycle, Sine wave, 50Hz Tvj = 25°C	I _{TSM}	500	A
I ² t value for fusing		I ² t	1250	A ² s
Critical rate of rise of on-state current	I _G =2×I _{GT}	di/dt	150	A/μs
RMS isolation voltage	A.C 50Hz(1s/1min)	V _{ISO}	3000/2500	V
Junction temperature range		T _J	-40 ~ +125	°C
Storage temperature range		T _{stg}	-40 ~ +125	°C

Table 6: Static Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Test Conditions	Symbol	Limits			Unit
			a	b	c	
Peak forward voltage	$I_T=75\text{A}$, $t_p=380\mu\text{s}$	V_T			1.90	V
Repetitive peak off-state current	$V_D = V_{\text{DRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{DRM}			500	μA
	$V_D = V_{\text{DRM}}$, $T_{vj} = 125^\circ\text{C}$				10	mA
Reverse leakage current	$V_R = V_{\text{RRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{RRM}			500	μA
	$V_R = V_{\text{RRM}}$, $T_{vj} = 125^\circ\text{C}$				10	mA
Threshold voltage	For power loss calculation only $T_{vj} = 125^\circ\text{C}$,	V_{TO}			1.0	V
Dynamic resistance	$T_{vj} = 125^\circ\text{C}$,	r_T			8	m Ω
Triggering gate current	$V_D=12\text{V}$ $R_L=30\Omega$	I_{GT}	20		120	mA
Holding current	$I_T=1\text{A}$	I_H			150	mA
Latching current	$I_G=1.2 I_{\text{GT}}$	I_L			300	mA
Critical rate of rise of voltage	$V_D=2/3V_{\text{DRM}}$ $T_{vj}=125^\circ\text{C}$ Gate Open	dv/dt	1000			V/ μs
Triggering gate voltage	$V_D=12\text{V}$ $R_L=30\Omega$	V_{GT}			1.5	V
Non triggering gate voltage	$V_D=V_{\text{DRM}}$ $T_{vj}=125^\circ\text{C}$	V_{GD}	0.2			V

Table 6: Thermal Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Test Conditions	Symbol	Limits			Unit
			a	b	c	
Thermal resistance, junction to case	per Thyristor	$R_{\text{th(j-c)}}$		1.2		/W
Mounting torque	Module torque to heatsink	M	1.8		2.0	N m

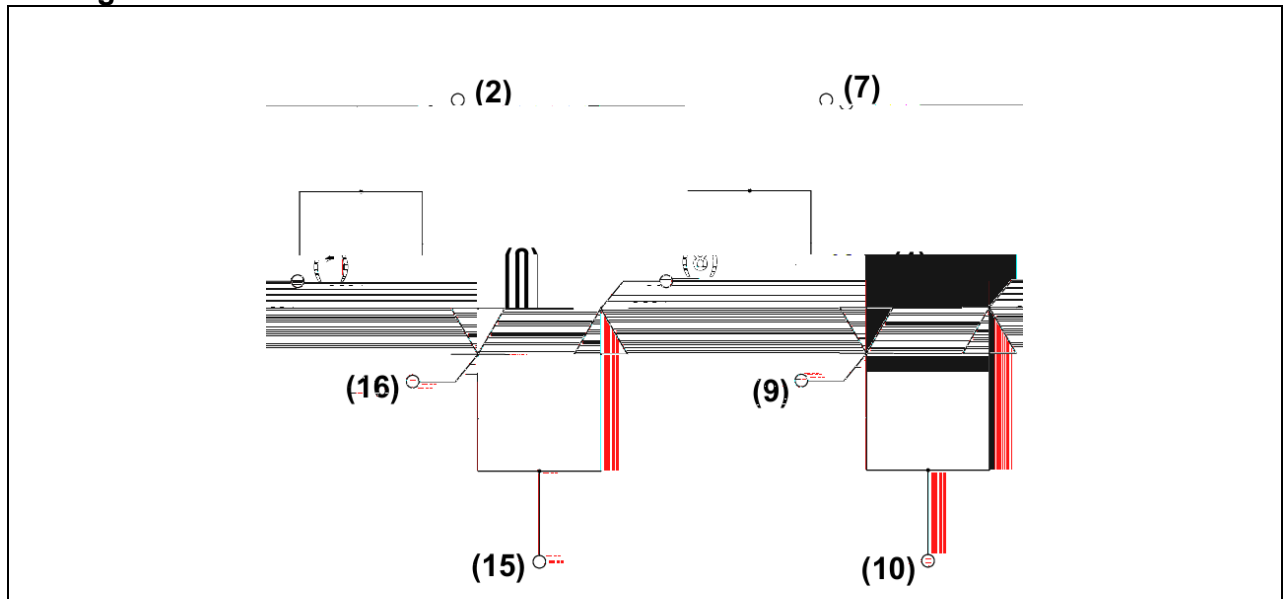


BeWea aYe Tgba

Xi VX	Te a	CTV T X	J X g	aaXe5bk	CXe6 Tgba
JMT50WT16S2C	JMT50WT16S2C	S2	16.8g/PCS	90 PCS	810 PCS

G c VT XVe VT G Xe T 6 TeTVXe f g Vf

6 eVh g T eT



CTV T XBhg aXf

